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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,593	09/29/2003	Ichiro Yokokura	1614.1363	8553

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EXAMINER	
ODOM, CURTIS B	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/671,593	YOKOKURA ET AL.	
	Examiner	Art Unit	
	Curtis B. Odom	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5 and 6* is/are rejected.

7)☒ Claim(s) *2-4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-6 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 5, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itoh (U. S. Patent No. 6, 233, 297) in view of Garlepp et al. (previously cited in Office Action 10/31/2006).

Regarding claim 1, Itoh discloses a digital phase locked circuit (see Fig. 2) for synchronizing a phase of an output clock signal with a phase of an input clock signal wherein the output clock signal is generated by dividing a master clock signal, comprising:

a phase comparing part (Fig. 2, block 4, see column 5, lines 39-44) comparing the phase of the output clock signal (output from 3-2) with the phase of the input clock signal (output from 3-1);

a phase comparison result detecting part (Fig. 2, block 5) outputting an INC/DEC request signal (I1, D2) based on a phase comparison signal from the phase comparing part;

an execution rate computing part (see Fig. 2, block 6-10) computing a phase difference (in the secondary random walk filter) between the input clock signal and the output clock signal as described in column 5, line 63-column 6, line 5) based on the INC/DEC (I1, D1) request signal from the phase comparison result detecting part and outputting an execution rate from the adder-subtractor corresponding to the phase difference as described in column 6, lines 18-37; and

a clock generating part (see Fig. 2, block 1) for changing phase absorption speed of the output clock signal regulating the frequency of the output clock signal (see column 5, lines 28-31) by adding and subtracting pulses from the output clock signal and by masking the INC/DEC request signal (as described in column 6, lines 32-37) depending on the execution rate computed in the adder-subtractor.

Itoh does not disclose the phase comparison result detecting part and the clock generating part controlling a division operation of the master clock signal in accordance with the INC/DEC request signal form the phase comparison result detecting part.

However, Garlepp et al. discloses a phase locked loop (see Fig. 7) which comprises of a control part including a phase compare logic (see Fig. 7, block 704) for comparing an output clock from a divider (Fig. 7, block 420) and an input clock (B). If the magnitude of the phase difference between the clocks is greater than a certain value, the phase compare logic asserts a spit/swallow (INC/DEC) control signal to control the execution rate of the divider in order to provide an output clock signal one clock cycle early or one clock cycle late (see column 7, lines 47-59). Therefore, it would have been obvious to one skilled in the art at the time the invention

was made to modify the phase locked loop of Itoh to control the execution rate of the divider as disclosed by Garlepp et al. since Garlepp et al. states the phase adjustment provided by the control of the execution rate of the divider allows the operation of the phase detector well within its linear range (see column 8, lines 13-17).

Regarding claim 5, Itoh discloses a digital phase locked circuit (see Fig. 2) for synchronizing a phase of a divided clock signal with a phase of an input clock signal wherein the divided clock signal is generated by dividing a master clock signal (Reference clock signal), comprising:

a phase comparing part (Fig. 2, block 4, see column 5, lines 39-44) comparing the phase of the output clock signal (output from 3-2) with the phase of the input clock signal (output from 3-1);

a phase comparison result detecting part (Fig. 2, block 5) referring to a comparison result from the phase comparing part and outputting an INC/DEC request signal (I1, D2);

a mask processing part (see Fig. 2, block 6-10) identifying a single applied mask rate among a plurality of mask rates as described in column 6, lines 18-37 for masking part of an INC/DEC (I1, D1) request signal depending on a phase difference between the input clock and the master clock signal generated in Fig. 2, block 4 (see column 5, lines 39-44) and Fig. 2, block 6 (see column 5, line 63-column 6, line 5), masking the output signal (I1, D1) from the phase comparison result detecting part (as described in column 6, lines 23-37) depending on the identified mask rate from the adder-subtractor (see column 6, lines 18-22), and outputting the masked signal (see column 6, line 23-37).

Itoh does not disclose the phase comparison result detecting part outputting a signal for increasing/decreasing a division number for dividing the master clock signal when the phase of the output clock signal proceeds forward/behind the phase of the input clock signal, wherein the divided clock signal is obtained by controlling increasing or decreasing operation on the division number based on the outputted masked signal.

However, Garlepp et al. discloses a phase locked loop (see Fig. 7) which comprises of a control part including a phase compare logic (see Fig. 7, block 704) for comparing an output clock from a divider (Fig. 7, block 420) and an input clock (B). If the magnitude of the phase difference between the clocks is greater than a certain value, the phase compare logic asserts a spit/swallow (masked INC/DEC) control signal to control the execution rate (division number) of the divider in order to provide an output clock signal one clock cycle early or one clock cycle late (see column 7, lines 47-59). The spit/swallow control signal is based on the output clock signal leading/lagging (in phase) in the input clock signal (see column 2, lines 42-59). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the phase locked loop of Itoh to control the execution rate of the divider based on the spit/swallow (masked) signal as disclosed by Garlepp et al. since Garlepp et al. states the phase adjustment provided by the control of the execution rate of the divider allows the operation of the phase detector well within its linear range (see column 8, lines 13-17).

Regarding claim 6, Itoh discloses a digital phase locked circuit (see Fig. 2) for synchronizing a phase of an output clock signal with a phase of an input clock signal wherein the output clock signal is generated by dividing a master clock signal, comprising:

a phase comparing part (Fig. 2, block 4, see column 5, lines 39-44) comparing the phase of the output clock signal (output from 3-2) with the phase of the input clock signal (output from 3-1);

a phase comparison result detecting part (Fig. 2, block 5) outputting an INC/DEC request signal (I1, D1) based on a phase comparison signal from the phase comparing part;

an execution rate computing part (see Fig. 2, block 6-10) computing a phase difference (in the secondary random walk filter) between the input clock signal and the output clock signal as described in column 5, line 63-column 6, line 5) based on the INC/DEC (I1, D1) request signal from the phase comparison result detecting part and outputting an execution rate from the adder-subtractor corresponding to the phase difference as described in column 6, lines 18-37; and

a clock generating part (see Fig. 2, blocks 1 and 9) including an INC/DEC request mask control means (see Fig. 2, block 9) and a clock generating logic (see Fig. 2, block 1), the INC/DEC request mask control means masking the INC/DEC request signal (as described in column 6, lines 32-37) based on the execution rate computed in the adder-subtractor (see column 6, lines 18-37) to obtain a desired absorption characteristic by regulating the frequency of the output clock signal (see column 5, lines 28-31) by adding and subtracting pulses from the output clock signal, the clock generating logic generating the output signal (see column 5, lines 45-56) based on the masked INC/DEC request signal.

Itoh does not disclose the phase comparison result detecting part and the clock generating part controlling a division operation of the master clock signal in accordance with the INC/DEC request signal form the phase comparison result detecting part.

However, Garlepp et al. discloses a phase locked loop (see Fig. 7) which comprises of a control part including a phase compare logic (see Fig. 7, block 704) for comparing an output clock from a divider (Fig. 7, block 420) and an input clock (B). If the magnitude of the phase difference between the clocks is greater than a certain value, the phase compare logic asserts a spit/swallow (INC/DEC) control signal to control the execution rate of the divider in order to provide an output clock signal one clock cycle early or one clock cycle late (see column 7, lines 47-59). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the phase locked loop of Itoh to control the execution rate of the divider as disclosed by Garlepp et al. since Garlepp et al. states the phase adjustment provided by the control of the execution rate of the divider allows the operation of the phase detector well within its linear range (see column 8, lines 13-17).

Allowable Subject Matter

4. Claims 2-4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Curtis B. Odom whose telephone number is 571-272-3046. The examiner can normally be reached on Monday- Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Curtis Odom
May 12, 2007